Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A bipolar junction transistor, comprising:

a substrate;

a dielectric layer formed on the substrate;

an opening formed in the dielectric layer to expose a portion of the substrate;

a heavily doped polysilicon layer formed on a sidewall of the opening to define a self-aligned base region in the opening;

an intrinsic base doped region positioned in a bottom of the opening and within the self-aligned base region defined by the heavily doped polysilicon layer;

a spacer formed on the heavily doped polysilicon layer to define a self-aligned emitter region in the opening; and

an emitter conductivity layer being filled within the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the intrinsic base doped region.

[c2] 2. The bipolar junction transistor of claim 1, wherein the heavily doped polysilicon layer comprises a boron dopant with a dosage ranging from 1E19 to 1E21 atoms/

cm^2.

[c3] 3. The bipolar junction transistor of claim 1, wherein the substrate is a silicon substrate.

[c4] 4. The bipolar junction transistor of claim 1, wherein the substrate is a non-selective epitaxial silicon substrate.

[c5] 5. The bipolar junction transistor of claim 1, further comprising a salicide layer formed on the emitter conductivity layer.

[c6] 6. The bipolar junction transistor of claim 1, further comprising a selective implant collector (SIC) region formed in the substrate beneath the intrinsic base doped region.

[c7] 7. The bipolar junction transistor of claim 1, further comprising an extended conductivity layer formed on the dielectric layer to connect to the heavily doped polysilicon layer.

[c8] 8. The bipolar junction transistor of claim 7, further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer.

[c9] 9. The bipolar junction transistor of claim 7, wherein the extended conductivity layer is composed of in-situ

doped polysilicon.

[c10] 10. The bipolar junction transistor of claim 7, further comprising a salicide layer formed on the extended conductivity layer.

[c11] 11. The bipolar junction transistor of claim 1, wherein the substrate further comprises at least a deep isolation trench.

[c12] 12. The bipolar junction transistor of claim 11, wherein the substrate further comprises at least a channel stop region formed in the bottom of the deep isolation trench.

[c13] 13. The bipolar junction transistor of claim 1, wherein the intrinsic base doped region comprises a boron dopant.

[c14] 14. A bipolar junction transistor, comprising:
a substrate;
a dielectric layer formed on the substrate;
an opening formed in the dielectric layer to expose a portion of the substrate;
a doped polysilicon layer formed on a sidewall of the opening and on the dielectric layer outside of the opening, the doped polysilicon layer defining a self-aligned base region in the opening;

an intrinsic base doped region positioned in a bottom of the opening and within the self-aligned base region defined by the doped polysilicon layer;
a spacer formed on the doped polysilicon layer to define a self-aligned emitter region in the opening; and
an emitter conductivity layer being filled within the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the intrinsic base doped region.

[c15] 15. The bipolar junction transistor of claim 14, wherein the doped polysilicon layer comprises a boron dopant.

[c16] 16. The bipolar junction transistor of claim 14, further comprising a salicide layer formed on the emitter conductivity layer and on the portion of the doped polysilicon layer outside of the opening.

[c17] 17. The bipolar junction transistor of claim 14, further comprising a selective implant collector (SIC) region formed in the substrate beneath the intrinsic base doped region.

[c18] 18. The bipolar junction transistor of claim 14, wherein the substrate further comprises at least a deep isolation trench.

[c19] 19. The bipolar junction transistor of claim 18, wherein

the substrate further comprises at least a channel stop region formed in the bottom of the deep isolation trench.

[c20] 20. The bipolar junction transistor of claim 14, wherein the intrinsic base doped region comprises a boron dopant.